What is claimed is:

1. A method of defining an integrated circuit layout for non-Manhattan elements using a Manhattan grid system, the method comprising the steps of:

a) determining the minimum grid resolution of a specific Manhattan layout and mask making system;

b) defining a minimum spacing between adjacent vertices of a polygon as the distance between a pair of selected grid points;

c) superimposing a non-Manhattan element over the Manhattan grid system;

d) fitting a plurality of polygons within the defined space of the non-Manhattan element by locating at least one vertex of each polygon on the periphery of the non-Manhattan element.

2. The method as defined in claim 1 wherein in performing step b), the selected pair of grid points are adjacent grid points.

3. The method as defined in claim 1 wherein the non-Manhattan element is a curved line and a plurality of inscribed rectangles are used to define the curve.

4. The method as defined in claim 1 wherein the non-Manhattan element is a curved line and a plurality of circumscribed rectangles are used to define the curve.

5. The method as defined in claim 1 wherein the non-Manhattan element is an optical element.

6. The method as defined in claim 5 wherein Manhattan-shaped electrical elements are included on the same grid as the non-Manhattan optical elements, allowing for both optical and electrical elements to be laid out simultaneously.

7. The method as defined in claim 1 wherein in performing step b), a rectangle is used as the polygon and the step includes defining minimum rectangle width as the distance between the pair of selected grid points.

8. The method as defined in claim 1 wherein the geometry of the non-Manhattan element is determined by using as an input an equation of a predetermined geometrical shape.

9. The method as defined in claim 1 wherein in performing step d), a plurality of vertices of at least one polygon are located on the periphery of the non-Manhattan element.

10. The method as defined in claim 1 wherein in performing step c), a diffractive optical element is superimposed over the Manhattan grid system.

11. A method for generating an integrated circuit layout of at least one non-Manhattan optical element and at least one Manhattan electronic element, the method comprising the steps of:

simulating a set of predetermined optical functions to generate a physical layout of at least one non-Manhattan optical element;

converting the physical layout of the at least one non-Manhattan optical element into a layout compatible with a Manhattan grid system, the converting step requiring the steps of:

a) determining the minimum grid resolution of a specific Manhattan layout and mask making system;

b) defining a minimum spacing between adjacent vertices of a polygon as the distance between a pair of selected grid points;

c) superimposing a non-Manhattan element over the Manhattan grid system;

d) fitting a plurality of polygons within the defined space of the non-Manhattan element by locating at least one vertex of each polygon on the periphery of the non-Manhattan element;

simulating a set of predetermined electrical functions to generate a physical layout of at least one Manhattan electronic element;

providing the Manhattan layout of the at least one electronic element and the converted Manhattan layout of the at least one optical element as inputs to a mask making system; and

generating a mask including the layout of both the optical and electronic elements on a Manhattan grid system.

12. A system for defining an integrated circuit layout for non-Manhattan elements using a Manhattan grid system, the system including a processor capable of performing the operations of

a) determining the minimum grid resolution of a specific Manhattan layout and mask making system;

b) defining a minimum spacing between adjacent vertices of a polygon as the distance between a pair of selected grid points;

c) superimposing a non-Manhattan element over the Manhattan grid system;

d) fitting a plurality of polygons within the defined space of the non-Manhattan element by locating at least one vertex of each polygon on the periphery of the non-Manhattan element.

13. The system as defined in claim 12 wherein the system further comprises an electronic IC layout tool for providing a layout of Manhattan elements, the output of the electronic IC layout tool provided as an input to the system processor for developing a single mask including both optical and electronic components.

14. A mask layout software tool comprising:

an optical simulator for developing a physical layout of at least one optical component having a non-Manhattan geometry;

a layout conversion module for converting the physical layout of the at least one optical component having a non-Manhattan geometry into a layout for use with a Manhattan grid system, the layout conversion module comprising a processor capable of performing the operations of:

a) determining the minimum grid resolution of a specific Manhattan layout and mask making system;

b) defining a minimum spacing between adjacent vertices of a polygon as the distance between a pair of selected grid points;

c) superimposing a non-Manhattan element over the Manhattan grid system;

d) fitting a plurality of polygons within the defined space of the non-Manhattan element by locating at least one vertex of each polygon on the periphery of the non-Manhattan element;

an electronic simulator for developing a physical layout of at least one electronic component having a Manhattan; and

a mask layout module, coupled to the electronic simulator and the output of the layout conversion module for generating a layout of both the optical and electrical components.